UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/507,213	03/28/2005	Dietmar Birgel	BIRG3004FJD	5089

23364 7590 02/04/2008

BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314

EXAMINER	
ABOAGYE, MICHAEL	
ART UNIT	**PAPER NUMBER**
1793	
MAIL DATE	**DELIVERY MODE**
02/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/507,213	BIRGEL, DIETMAR	
	Examiner	Art Unit	
	Michael Aboagye	1793	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-53 and 61-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-53 and 61-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/28/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. The examiner acknowledges applicant's election without traverse to prosecute group I invention (claims 31-53, 61 and 64). Claims 62 and 63 depends on the independent claim 31 drawn to a method, and therefore would be examined together with the elected group.

Drawings

2. The drawings are objected to because figures 1-5 should be designated/labeled **Prior Art**. Also claims 4 and 6 are objected to for including **a language other than English.** Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 62 and 64 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 62 and 64 recite the limitations "above average amount of copper is provided" and "below average portion is provided" respectively. It is unclear as to what the applicant means by these limitations. No evidence has been provided by the applicant as to what portion of copper constitutes a baseline from which said comparisons are derived from. Said claims are therefore indefinite.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 31-38, 44,46,49,49, 52, 53,61and 63 are rejected under 35 U.S.C. 102(b) as being anticipated by Kenshi (EP 0469 788 A2).

Kenshi teaches a method for populating and soldering a circuit board having a first side and a second side, populating electronic parts with lead wires of relatively low temperature resistance (the examiner interprets the relatively low temperature resistance components to be the same as THT-component) on the first side of the circuit board, with the connection wire or pin stuck from the first side through a hole and emerging on the second side of the circuit board in the area of a soldering contact surface printed with a solder paste; populating of the second side of the circuit board with the SMD-component and it is soldered, together with the electronic parts with lead wires, in the reflow oven (abstract, column 2, lines 25-35, column 2, line 51-column 3, line 51); wherein the first side populated with the electronic parts with lead wires is at least partially, shielded from a heat or energy feed effecting the soldering (column 3, lines 36-50 and column 4, lines 14-34). Regarding the, temperature difference of 28 degrees celsius, Kenshi teaches maintaining an appropriate temperature difference between the SMD component and the low temperature resistance components to prevent damaging the latter components (column 3, lines 10-15), and recites a temperature difference of about 300 degrees celsius (see, column 9, lines 34-44). Kenshi teaches aligning the circuit board with the components or parts on a conveyor and transporting or passing through the reflow oven during the soldering process (column 3, lines 30-40, Kenshi also teaches cooling the circuit board after reflow (column 9, lines 3-15 and column 12, lines 25-40). Kenshi teaches a reflow oven having coverings of metallic material such as steel at selected areas where excessive heating by the heat or energy feed effecting the soldering in the reflow oven is desired (column 4, lines 14-25, column 5, lines 25-32, and column 6, line 55-column 7, line 5). Kenshi

teaches a pin-in-hole component (component 7 with leads, see figures 3 and 11; column 9, lines 1-15)

7. Claims 31-37, 47 and 48 are rejected under 35 U.S.C. 102(b) as being anticipated by Updike et al. (US Patent No. 6,202,916).

Updike et al. teaches a method for populating and soldering a circuit board having a first side and a second side, populating electronic parts with lead wires of relatively low temperature resistance (the examiner interprets the relatively low temperature resistance components to be the same as THT-component) on the first side of the circuit board, with the connection wire or pin stuck from the first side through a hole and emerging on the second side of the circuit board in the area of a soldering contact surface printed with a solder paste; populating of the second side of the circuit board with the SMD-component and it is soldered, together with the electronic parts with lead wires, in the reflow oven (abstract, column 2, lines 10-38 and column 3, lines 27-30); wherein the first side populated with the electronic parts with lead wires is at least partially, shielded from a heat effecting the soldering by a pallet (item 14, figure 1); (column 2, line 63-column 4, line 13). Updike et al. also teaches the circuit board itself acting as a heat shield, and heat sink (item 20, figure 1) attached on the board (item 12 , figure 1) on a side of the soldering (see, figure 1, and column 3, lines 12-22 and lines 55-60).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 39-41 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenshi (EP 0469 788 A2) as applied to claim 31 and further in view of Berger (US Patent No. 4,515,304).

Kenshi do not expressly teach dressing the electronic parts with lead wires involving, shortening, crimping, clinching or bending the wire; applying adhesive to secure the component on the board prior to soldering.

Berger teaches a method for populating and soldering a circuit board having a first side and a second side, populating electronic parts with lead wires on a first side and a surface mounting component on the other side; attaching the leaded components by inserting the leads through the holes in the circuit board and the leads cut and clinched or crimped to prevent the components from falling out when the circuit board is inverted (Berger, abstract, column 2, lines 1-10, column 3, lines 1-37 and figures 1-9). Berger teaches attaching a surface mounting component initially by adhesive to secure them on the circuit board prior to reflow soldering (Berger, abstract). Berger teaches a pin-in-hole component (components 20 and 31, figures 1-9).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the method of Kenshi to dress the electronic parts having lead wires involving, shortening, crimping, clinching or bending the wire as taught by Berger to prevent the components from falling out when the circuit board is inverted (Berger, abstract, column 2, lines 1-10, column 3, lines 1-37 and figures 1-9).

10. Claims 42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenshi (EP 0469 788 A2) as applied to claim 31 and further in view of McGeorge (US Patent No. 4,200,900).

Kenshi fail to teach mechanically securing the leaded component by snap-in mechanism on the circuit board.

McGeorge teaches mounting electronic components on a circuit board; wherein the mounting pins, lead or wires are removably secured to the circuit board by snap lock arrangement (McGeorge, claim 4).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the method of Kenshi to mechanically secure leaded component by snap-in mechanism on the circuit board as taught by McGeorge so that said components can easily be removed or replaced (McGeorge, claim 4).

11. Claims 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenshi (EP 0469 788 A2) as applied to claim 31 and further in view of Aspandiar et al. (US Patent No. 6,651,869).

Kenshi does not expressly teach a non-metallic heat shield.

Aspandiar et al. teaches wave soldering a circuit board, wherein a non-metallic heat shield is used to protect a topside BGA component solder joint from reflow during the wave soldering process (Aspandiar et al., column 2, lines 45-51 and figure 2).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the method of Kenshi to use a non-metallic heat shield as taught Aspandiar et al. to protect a topside BGA component solder joint

from reflow during the wave soldering process (Aspandiar et al., column 2, lines 45-51 and figure 2).

13. Claims 62 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenshi (EP 0469 788 A2) as applied to claim 31 and further in view of Joshi (US Patent No. 6,294,403).

Kenshi does not expressly teach using copper layer on the surface of the circuit board to regulate heat uptake or dissipation.

Joshi teaches a forming a circuit board assembly and providing a covering or a layer of copper on the surface of the circuit board (Joshi, column 1, lines 36-49).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the method of Kenshi to provide cover covering or layer on the surface of the circuit board as taught by Joshi to serve as a means of regulating the heat uptake or dissipation during the furnace reflow process (Joshi, column 1, lines 36-49).

14. Claims 39-41 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Updike et al. (US Patent No. 6,202,916) as applied to claim 31 and further in view of Berger (US Patent No. 4,515,304).

Updike et al. do not expressly teach dressing the electronic parts with lead wires involving, shortening, crimping, clinching or bending the wire; applying adhesive to secure the component on the board prior to soldering.

Berger teaches a method for populating and soldering a circuit board having a first side and a second side, populating electronic parts with lead wires on a first side and a surface mounting component on the other side; attaching the leaded components by inserting the leads through the holes in the circuit board and the leads cut and clinched or crimped to prevent the components from falling out when the circuit board is inverted (Berger, abstract, column 2, lines 1-10, column 3, lines 1-37 and figures 1-9). Berger teaches attaching a surface mounting component initially by adhesive to secure them on the circuit board prior to reflow soldering (Berger, abstract). Berger teaches a pin-in-hole component (components 20 and 31, figures 1-9).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the method of Updike et al. to dress the electronic parts with lead wires involving, shortening, crimping, clinching or bending the wire as taught by Berger to prevent the components from falling out when the circuit board is inverted (Berger, abstract, column 2, lines 1-10, column 3, lines 1-37 and figures 1-9).

15. Claims 42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Updike et al. (US Patent No. 6,202,916) as applied to claim 31 and further in view of McGeorge (US Patent No. 4,200,900).

Updike et al. fail to teach mechanically securing the leaded component by snap-in mechanism on the circuit board.

McGeorge teaches mounting electronic components on a circuit board; wherein the mounting pins, lead or wires are removably secured to the circuit board by snap lock arrangement (McGeorge, claim 4).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the method of Updike et al. to mechanically secure leaded component by snap-in mechanism on the circuit board as taught by McGeorge so that said components can easily be removed or replaced (McGeorge, claim 4).

16. Claims 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Updike et al. (US Patent No. 6,202,916) as applied to claim 31 and further in view of Aspandiar et al. (US Patent No. 6,651,869).

Updike et al. does not expressly teach a non-metallic heat shield.

Aspandiar et al. teaches wave soldering a circuit board, wherein a non-metallic heat shield is used to protect a topside BGA component solder joint from reflow during the wave soldering process (Aspandiar et al., column 2, lines 45-51 and figure 2).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the method of Updike et al. to use a non-metallic heat shield as taught Aspandiar et al. to protect a topside BGA component solder joint from reflow during the wave soldering process (Aspandiar et al., column 2, lines 45-51 and figure 2).

17. Claims 62 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Updike et al. (US Patent No. 6,202,916) as applied to claim 31 and further in view of Joshi (US Patent No. 6,294403).

Updike et al. does not expressly teach using copper layer on the surface of the circuit board to regulate heat uptake or dissipation.

Joshi teaches a forming a circuit board assembly and providing a covering or a layer of copper on the surface of the circuit board (Joshi, column 1, lines 36-49).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the method of Updike et al. to provide cover covering or layer on the surface of the circuit board as taught by Joshi to serve as a means of regulating the heat uptake or dissipation during the furnace reflow process (Joshi, column 1, lines 36-49).

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Margins et al. (US 4,982,376), and Thompson, Sr. (US 5,704,535) are also cited in PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Aboagye whose telephone number is 571-272-8165. The examiner can normally be reached on Mon - Fri 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jonathan Johnson can be reached on 571-272-1177. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael Aboagye
Assistant Examiner
Art Unit 1793
01/27/2008

AM
AM

JONATHAN JOHNSON
SUPERVISORY PATENT EXAMINER